



浙江大学
ZheJiang University

Computer Architecture ----A Quantitative Approach

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2014/4/13

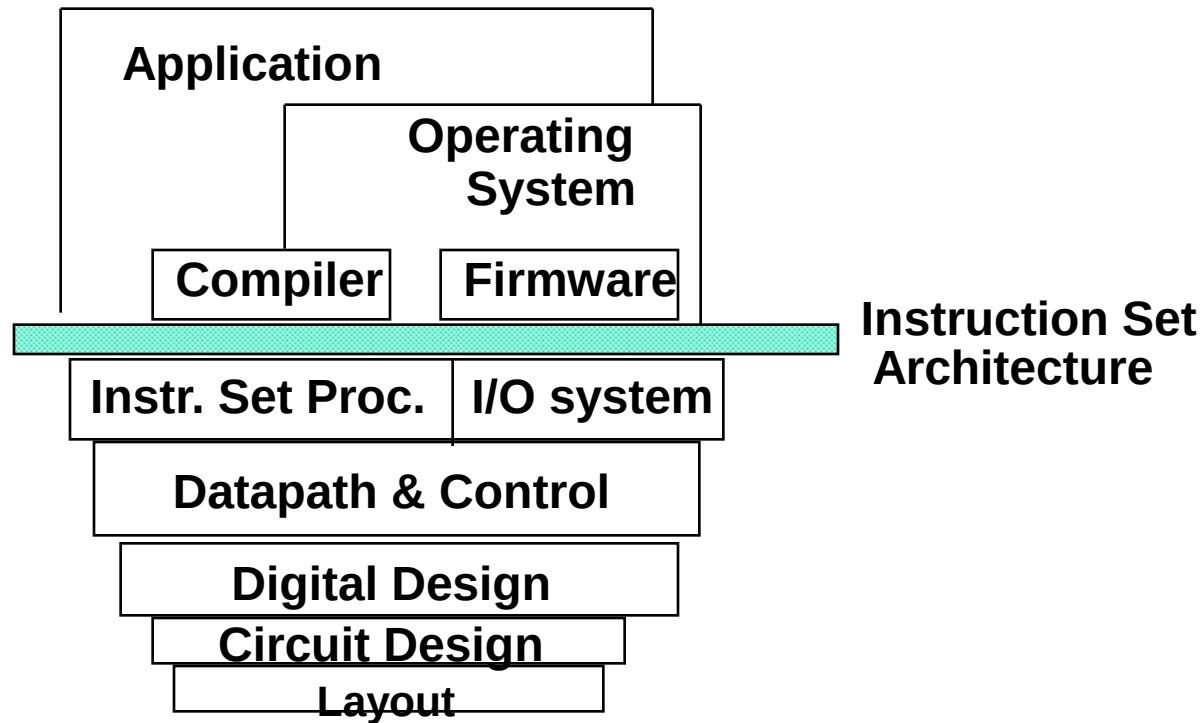


What is Computer Architecture





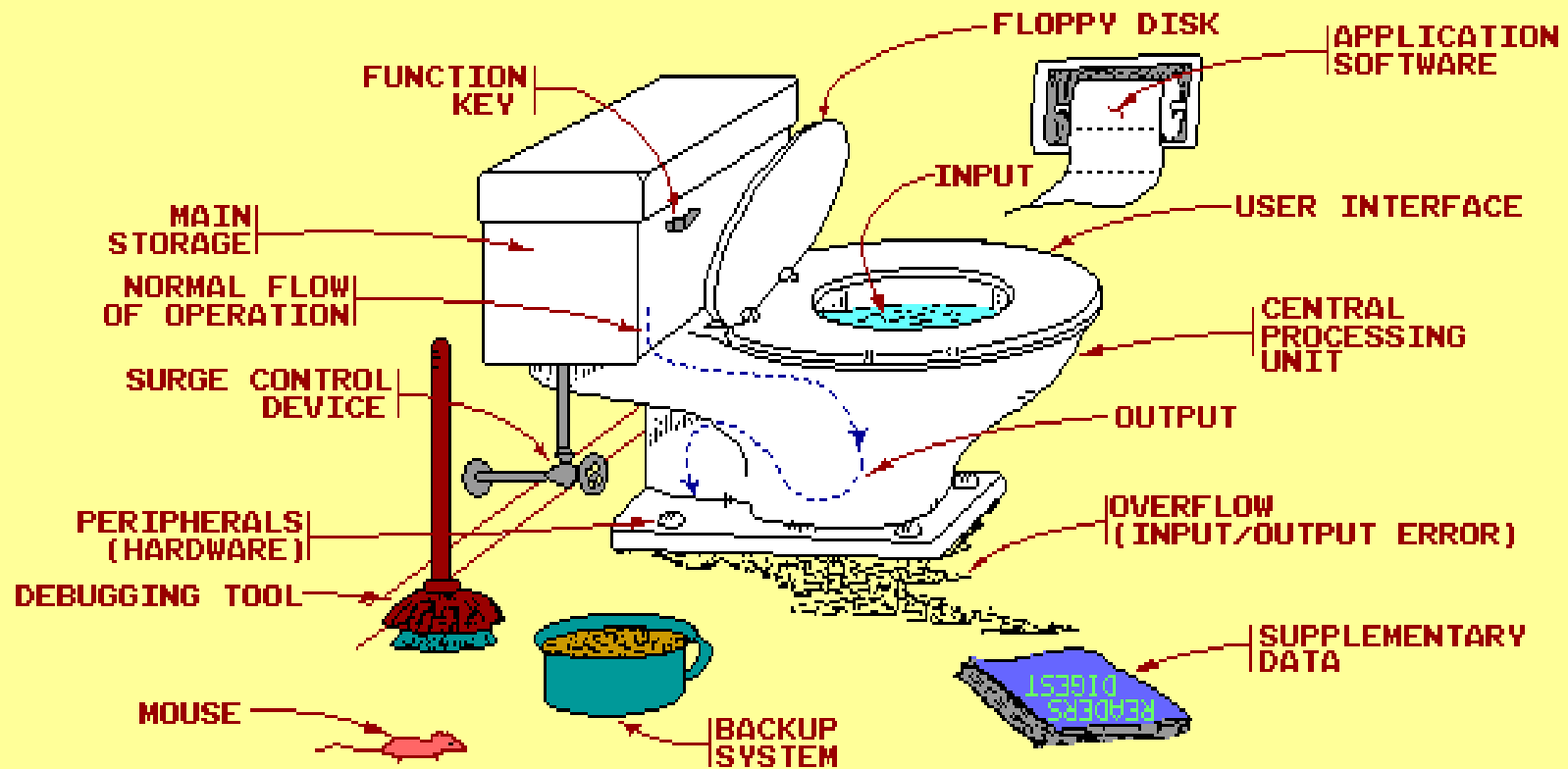
What is Computer Architecture





What is Computer Architecture

Understanding the Technology





What is Computer Architecture

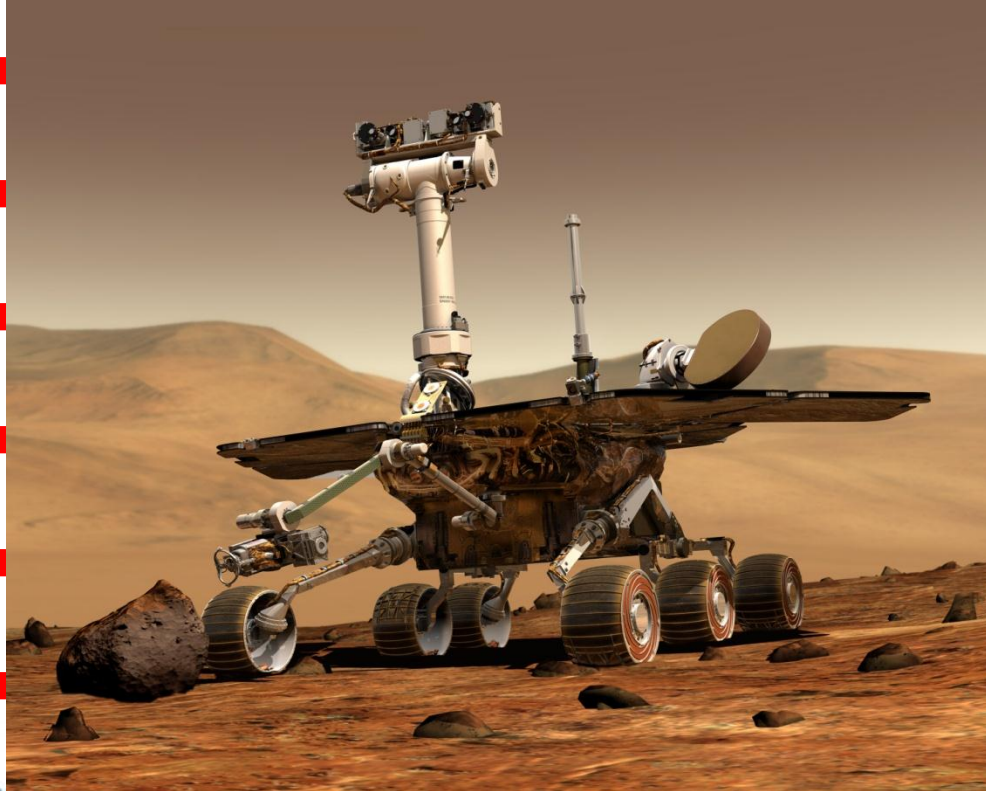
- Difference with Instruction Set
- Difference with Computer Organization
- Difference with Computer Implementation
- Categories of Computer science





Recent research fields

- Develop
process



echip;

tem

Architecture
rchitecture





- on-chip multilevel cache&pre-fetch buffer
- Context switch by hardware
- Massive on-chip DRAM
- **Depth pipeline** 8-12→ 20
- Advanced Super-scalar: 16-32 instr/clock cycle
- **Super-speculative** Processor: fine-grain heavy speculation
- Trace Processor
- Vector Intelligent RAM Procссор, V-IRAM
- on-chip multiprocessor
- Instruction-level Distributed Processing (ILDP)
- Clustered Dependence-based Architecture



- Mult-processor architecture based on micro-processor
- Availability maintainability scalability
 - HA
 - RAID
 - Reconfigurable





- New apparatus to make processor
 - Light computer
 - Molecule computer
 - DNA computer





Top500, HPC

Rank	Site	Computer
1	DOE/NNSA/LANL United States	Roadrunner - BladeCenter QS22/LS21 Cluster, PowerXCell 8i 3.2 Ghz / Opteron DC 1.8 GHz , Voltaire Infiniband IBM
2	Oak Ridge National Laboratory United States	Jaguar - Cray XT5 QC 2.3 GHz Cray Inc.
3	NASA/Ames Research Center/NAS United States	Pleiades - SGI Altix ICE 8200EX, Xeon QC 3.0/2.66 GHz SGI
4	DOE/NNSA/LLNL United States	BlueGene/L - eServer Blue Gene Solution IBM
5	Argonne National Laboratory United States	Blue Gene/P Solution IBM
6	Texas Advanced Computing Center/Univ. of Texas United States	Ranger - SunBlade x6420, Opteron QC 2.3 Ghz, Infiniband Sun Microsystems
7	NERSC/LBNL United States	Franklin - Cray XT4 QuadCore 2.3 GHz Cray Inc.
8	Oak Ridge National Laboratory United States	Jaguar - Cray XT4 QuadCore 2.1 GHz Cray Inc.
9	NNSA/Sandia National Laboratories United States	Red Storm - Sandia/ Cray Red Storm, XT3/4, 2.4/2.2 GHz dual/quad core Cray Inc.
10	Shanghai Supercomputer Center China	Dawning 5000A - Dawning 5000A, QC Opteron 1.9 Ghz, Infiniband, Windows HPC 2008 Dawning



TOP 10, 11/2009

1	<u>Jaguar - Cray XT5-HE Opteron Six Core 2.6 GHz</u>
2	<u>Roadrunner - BladeCenter QS22/LS21 Cluster, PowerXCell 8i 3.2 Ghz / Opteron DC 1.8 GHz, Voltaire Infiniband</u>
3	<u>Kraken XT5 - Cray XT5-HE Opteron Six Core 2.6 GHz</u>
4	<u>JUGENE - Blue Gene/P Solution</u>
5	<u>Tianhe-1 - NUDT TH-1 Cluster, Xeon E5540/E5450, ATI Radeon HD 4870, Infiniband</u>
6	<u>Pleiades - SGI Altix ICE 8200EX, Xeon QC 3.0 GHz/Nehalem EP 2.93 Ghz</u>
7	<u>BlueGene/L - eServer Blue Gene Solution</u>
8	<u>Blue Gene/P Solution</u>
9	<u>Ranger - SunBlade x6420, Opteron QC 2.3 Ghz, Infiniband</u>
10	<u>Red Sky - Sun Blade x6275, Xeon X55xx 2.93 Ghz, Infiniband</u>



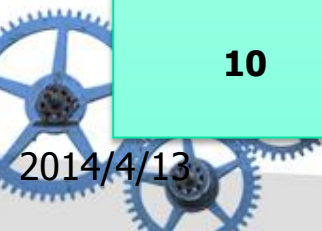
TOP 10, 11/2010

1	<u>Tianhe-1A - NUDT TH MPP, X5670 2.93Ghz 6C, NVIDIA GPU, FT-1000 8C</u>
2	<u>Jaguar - Cray XT5-HE Opteron 6-core 2.6 GHz</u>
3	<u>Nebulae - Dawning TC3600 Blade, Intel X5650, NVidia Tesla C2050 GPU</u>
4	<u>TSUBAME 2.0 - HP ProLiant SL390s G7 Xeon 6C X5670, Nvidia GPU, Linux/Windows</u>
5	<u>Hopper - Cray XE6 12-core 2.1 GHz</u>
6	<u>Tera-100 - Bull bullx super-node S6010/S6030</u>
7	<u>Roadrunner - BladeCenter QS22/LS21 Cluster, PowerXCell 8i 3.2 Ghz / Opteron DC 1.8 GHz, Voltaire Infiniband</u>
8	<u>Kraken XT5 - Cray XT5-HE Opteron 6-core 2.6 GHz</u>
9	<u>JUGENE - Blue Gene/P Solution</u>
10	<u>Cielo - Cray XE6 8-core 2.4 GHz</u>



TOP 10, 11/2011

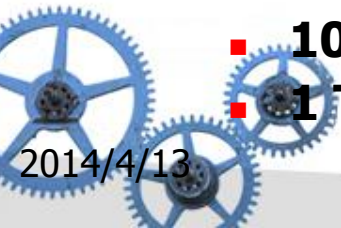
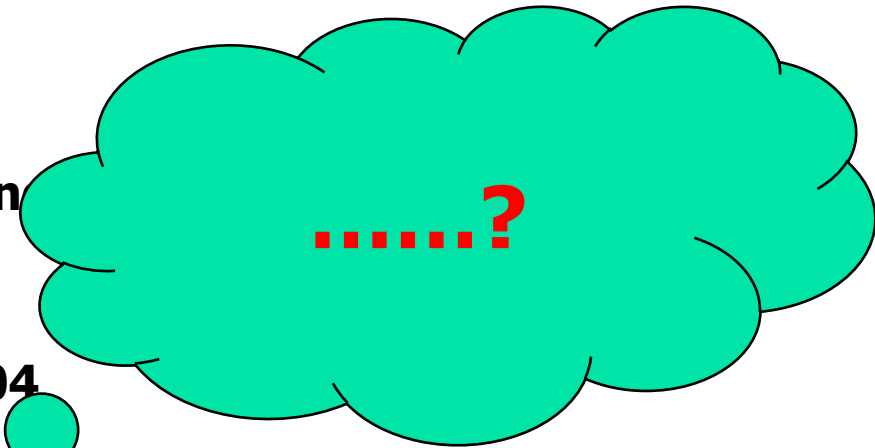
1	<u>K computer, SPARC64 VIIIfx 2.0GHz, Tofu interconnect</u>
2	<u>NUDT YH MPP, Xeon X5670 6C 2.93 GHz, NVIDIA 2050</u>
3	<u>Cray XT5-HE Opteron 6-core 2.6 GHz</u>
4	<u>Dawning TC3600 Blade, Intel X5650, NVidia Tesla C2050 GPU</u>
5	<u>HP ProLiant SL390s G7 Xeon 6C X5670, Nvidia GPU, Linux/Windows</u>
6	<u>Cray XE6, Opteron 6136 8C 2.40GHz, Custom</u>
7	<u>SGI Altix ICE 8200EX/8400EX, Xeon HT QC 3.0/Xeon 5570/5670 2.93 Ghz, Infiniband</u>
8	<u>Cray XE6, Opteron 6172 12C 2.10GHz, Custom</u>
9	<u>Bull bullx super-node S6010/S6030</u>
10	<u>BladeCenter QS22/LS21 Cluster, PowerXCell 8i 3.2 Ghz / Opteron DC 1.8 GHz, Voltaire Infiniband</u>





Fastest computer in China

- **2011:**
 - **TianHe-1A 2.57 petaflop/s**
- **2009**
 - **TianHe-1**
- **2008 ShuGuang5000A**
 - **180.6 TeraFlops**
 - **122.88TB RAM, 30720 computing nodes**
- **2004 ShuGuang4000A**
 - **11 TeraFLOPS**
 - **rank 10 in top 500 in June, 2004**
- **2003 ShenTeng6800**
 - **5.324 TeraFLOPS**
- **2002 ShenTeng1800**
 - **2.04 TeraFLOPS**
- **2000 YinHe IV**
 - **1024 CPU**
 - **1 TeraFLOPS**





Why ?

- Where there is a will, there is a way.





Top conference in CA

- **ISCA:** The International Symposium on Computer Architecture
- **MICRO:** Intl Symp on Microarchitecture
- **OSDI**、**SOAP**、**HPCA**、**ASPLOS**.....





Eckert-Mauchly Award

2011	<u>Sohi, Gurindar S</u>	1994	<u>Thornton, James E.</u>
2010	<u>Dally, William J</u>	1993	<u>Kuck, David J</u>
2009	<u>Emer, Joel</u>	1992	<u>Flynn, Michael J.</u>
2008	<u>Patterson, David</u>	1991	<u>Smith, Burton J.</u>
2007	<u>Valero, Mateo</u>	1990	<u>Batcher, Kenneth E.</u>
2006	<u>Pomerene, James H</u>	1989	<u>Cray, Seymour</u>
2005	<u>Colwell, Robert P.</u>	1988	<u>Siewiorek, Daniel P.</u>
2004	<u>Brooks, Frederick P.</u>	1987	<u>Amdahl, Gene M.</u>
2003	<u>Fisher, Joseph A. (Josh)</u>	1986	<u>Cragon, Harvey G</u>
2002	<u>Rau, B. Ramakrishna (Bob)</u>	1985	<u>Cocke, John</u>
2001	<u>Hennessy, John</u>	1984	<u>Dennis, Jack B.</u>
2000	<u>Davidson, Edward</u>	1983	<u>Kilburn, Tom</u>
1999	<u>Smith, James E.</u>	1982	<u>Bell, C. Gordon</u>
1998	<u>Watanabe, T.</u>	1981	<u>Clark, Wesley A.</u>
1997	<u>Tomasulo, Robert</u>	1980	<u>Wilkes, Maurice V.</u>
1996	<u>Patt, Yale</u>	1979	<u>Barton, Robert S.</u>
1995	<u>Crawford, John</u>		



Big Men in Architecture(1)

■ 2007 Mateo Valero

<http://personals.ac.upc.edu/mateo/>

For important contributions to instruction level parallelism and superscalar processor design.

MATEO VALERO

A portrait photograph of Mateo Valero, a man with short grey hair and a beard, wearing a light blue striped shirt and a dark tie.

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Department

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Fax: +34 - 93 401 70 55
e-mail: mateo@ac.upc.es
www.ac.upc.es





Big Men in Architecture(2)



■ 2001 Hennessy, John

For being the founder and chief architect of the MIPS Computer Systems and contributing to the development of the landmark **MIPS R2000** microprocessor.





Big Men in Architecture(3)



Frederick P. Brooks

<http://www.cs.unc.edu/~brooks/>

2004 Eckert-Mauchly Award

"For the definition of computer architecture and contributions to the concept of computer families and to the principles of instruction set design; for seminal contributions in instruction sequencing, including interrupt systems and execute instructions; and for contributions to the **IBM 360 instruction set architecture.**"

■ **1999 ACM Turing Award**

landmark contributions to computer architecture, operating systems, and software engineering."





Big Men in Architecture(4)

?!

1997 Robert Tomasulo

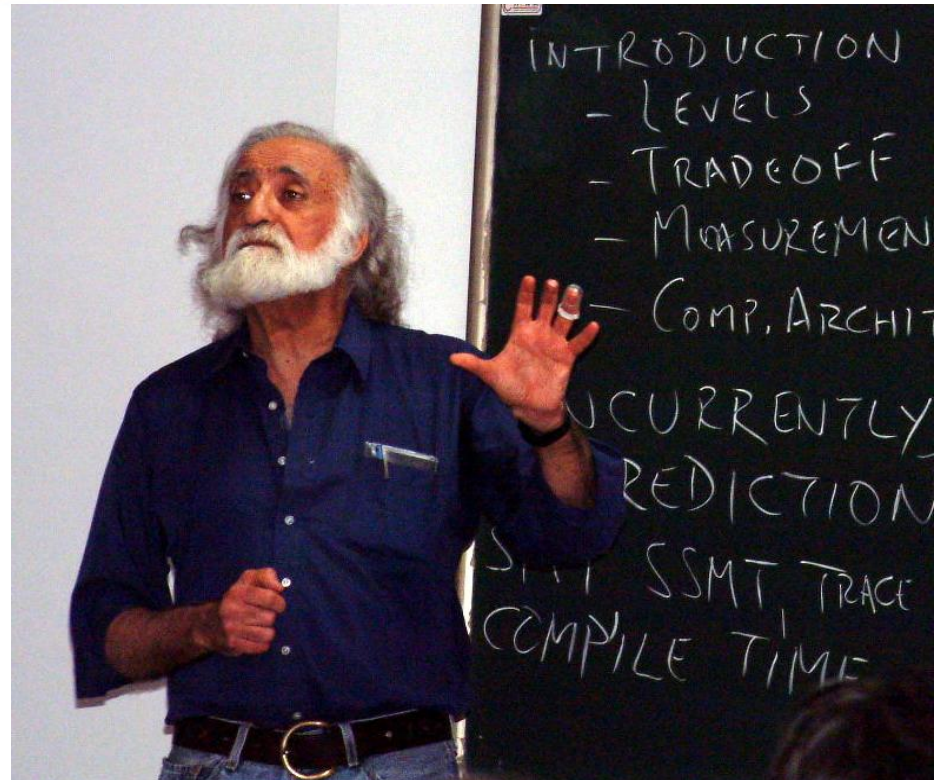
For the ingenious Tomasulo's algorithm, which enabled out-of-order execution processors to be implemented.





Big Men in Architecture(5)

- 1996 Yale Patt
For important contributions to instruction level parallelism and superscalar processor design.





Big Men in Architecture(6)

■ 1992 **Michael J. Flynn**

<http://www.cpe.calpoly.edu/IAB/flynn.html>

- For his important and seminal contributions to processor organization and classification, computer arithmetic and performance evaluation.



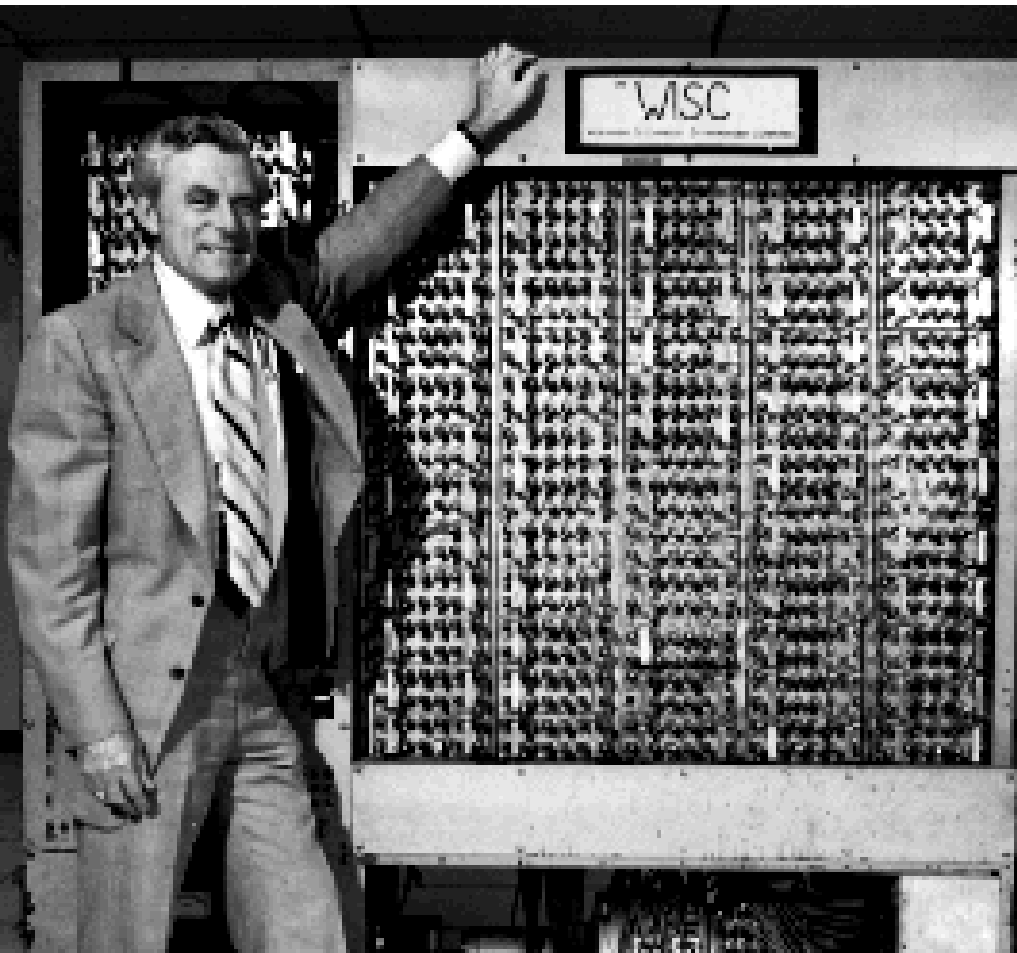


Big Men in Architecture(7)

- 1989 Cray, Seymour
- For a career of achievements that have advanced supercomputing design.



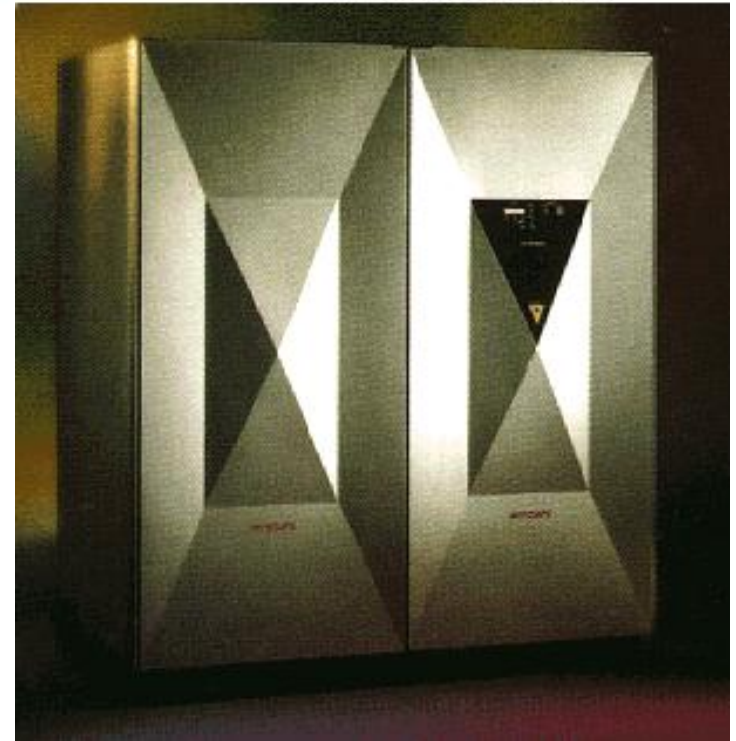
From Computer Desktop Encyclopedia
Reproduced with permission.
© 1999 Dr. Gene M. Amdahl



In 1975, Dr. Amdahl stands beside the Wisconsin Integrally Synchronized Computer (WISC), which he designed in 1950. It was built in 1952. (Image courtesy of Dr. Gene M. Amdahl.)

Architecture(8)

From Computer Desktop Encyclopedia
Reproduced with permission.
© 1997 Amdahl Corporation



ons in computer
belining, instruction
emory.



How ?

- Possibility:
 - standing on the shoulder of giants.
- Concepts, Ideas and Principles
- Quantitative approaches
- Hit the problem and right way to solve problem
- ***As a man sows, so he shall reap.***





Grading

- Class performance ~ 5%
- Pop quiz ~10%
- Reading ~10%
 - Write an summarize, no less than 3000 words
- Assignments ~10%
- Final examination ~35%
- Experiment ~35%

Close book !!
In English !!





Important Note about Grading

- Don't ask me for a higher score after the final examination **no matter what reason you have !**
- Otherwise you get **10% off** from your original score.





Assignments and reading

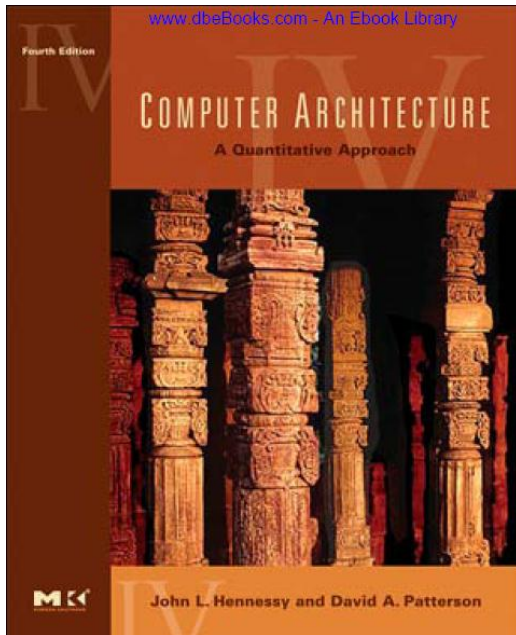
- Group work in assignments is permitted
- Group discussion is strongly encouraged
- Members in one group are no more than 3
- Homework need to be submitted in time.
- the more Late the more discount





Text Book

- Computer Architecture - A quantitative approach (4th edition or 3rd edition)
 - John L. Hennessy (Stanford University)
 - David A. Patterson (University of California, Berkeley)
 - China Machine Press,





David A. Patterson (UC Berkeley)





Reference-1

- Computer Architecture - A quantitative approach
 - (3rd edition , Chinese Version)
 - Translated by Zheng-WeiMin, Tang-ZhiZhong, etc
 - Publishing House of Electronics Industry
 - 郑伟民 汤志忠 汪东升等 , 电子工业出版社





Reference-2



- Computer Architecture -
A quantitative approach
 - (4rd edition , Chinese Version)
 - Translated by Bai-Yuebi etc
 - Publishing House of Electronics Industry
 - 白跃彬等 ,
电子工业出版社





What's new on this Edition ?

- Most significant edition:
 - 1~3 edition focus on ILP(Inst-Level Parallelism)
=>Focus on TLP(Thread-level parallelism) and DLP(Data-level parallelism).
- Chapter adjustment:
 - Changing technology
=>More emphasize on Dependability and topics of Power
- Book size limitation:
 - More contents move to Appendix and CD





Contents

- Ch1 Fundamentals of computer design
- Ch2 ILP and its exploitation
- Ch3 Limits of ILP
- **Ch4 Multiprocessor** and TLP
- Ch5 Memory Hierarchy Design
- **Ch6 Storage Systems**
- AppA Pipelining: Basic and Intermediate Concepts
- **AppB Instruction Set Principles and Examples**
- AppC Review of Memory Hierarchy
- AppD Embedded systems
- AppE Interconnection Networks
- **AppF Vector Processors**





Topics covered in this class

- Ch1 Fundamentals of computer design
- AppB Instruction Set Principles and Examples
- AppA Pipelining: Basic and Intermediate Concepts
- AppC Review of Memory Hierarchy
- Ch5 Memory Hierarchy Design
- Ch6 Storage Systems
- Ch4 Basic concepts of Multiprocessor
- AppF Vector Processors





What can you learn from this course ?





Course materials

- <http://10.71.45.100>
- WWW Computer Architecture Website:
 - <http://www.cs.wisc.edu/arch/www/>
- <http://www.csee.umbc.edu/~plusquel/611/index.html>
- <http://www.ece.cmu.edu/~ece347/>
- WWW Computer Architecture Page
 - <http://www.cs.wisc.edu/~arch/www/>





That's all for today !

Thank you !

