浙江大学
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Computer Architecture Experiment

Topic 4. Pipelined CPU with forwarding

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Outline

- Experiment Purpose
- Experiment Task
- Basic Principle
- Operating Procedures
- Precaution
- Checkpoints

Experiment Purpose

- Understand the principles of Pipelined CPU Bypass Unit
- Master the method of Pipelined Pipeline Forwarding Detection and Pipeline Forwards.
- Master the Condition In Which Pipeline Forwards.
- Master the Condition In Which Bypass Unit doesn't Work and the Pipeline stalls.
- master methods of program verification of Pipelined CPU with forwarding

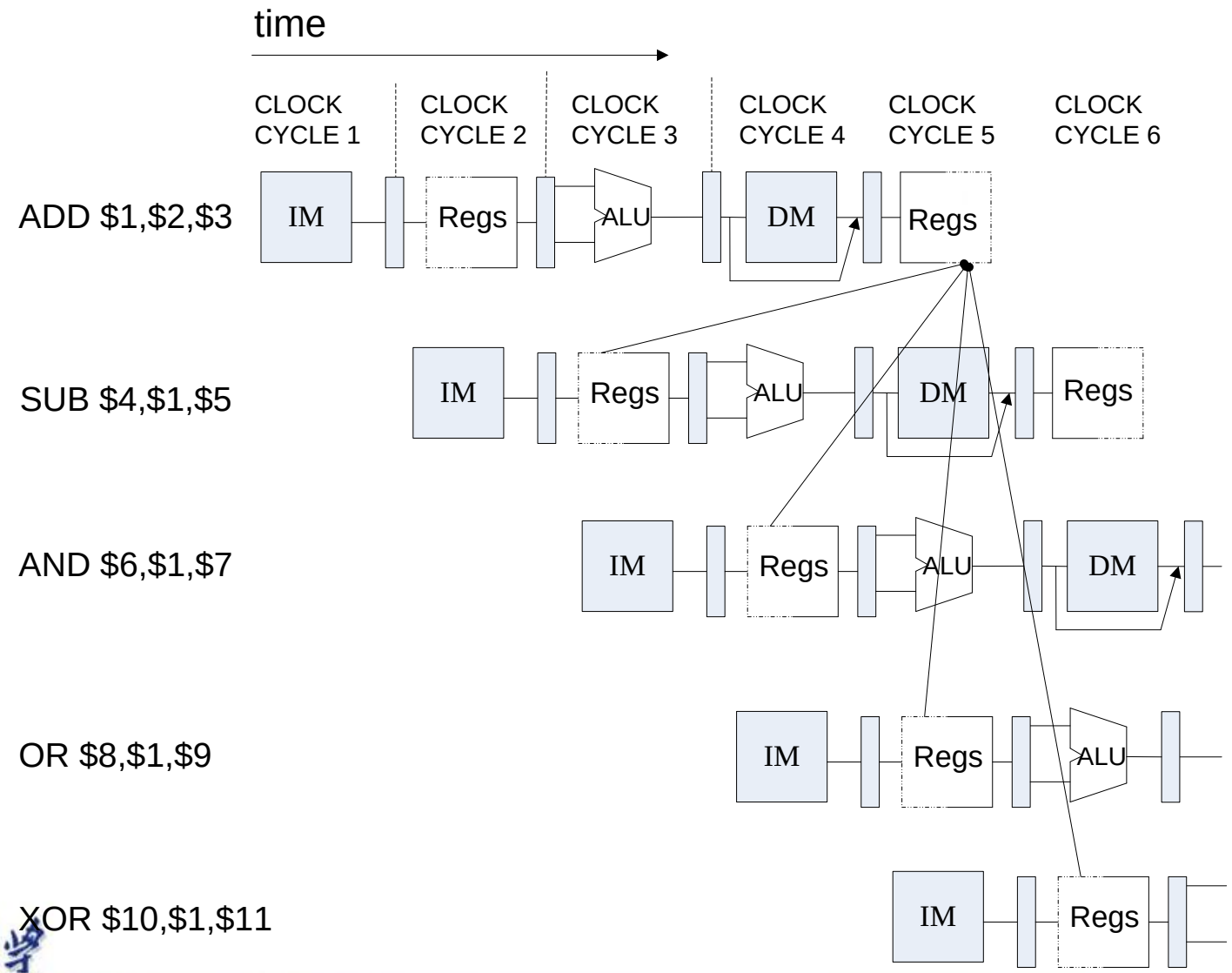
Experiment Task

- **Design the Bypass Unit of Datapath of 5-stages Pipelined CPU**
- **Modify the CPU Controller**
  - Conditions in Which Pipeline Forwards.
  - Conditions in Which Pipeline Stalls.
- **Verify the Pipeline CPU with program and observe the execution of program**

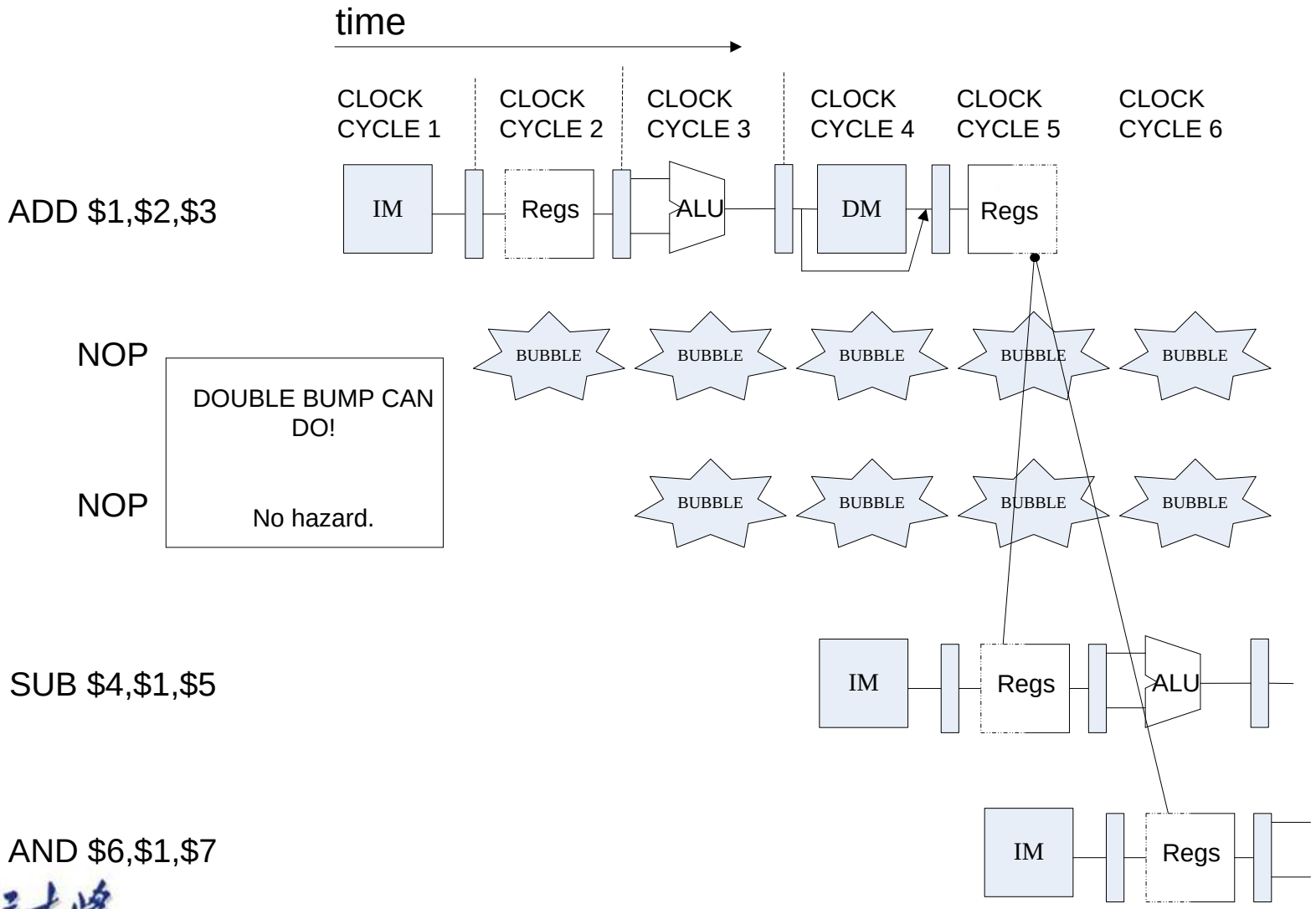
Data Hazard Stalls

- **Minimizing Data Hazard Stalls by Forwarding：In most cases, the problem can be resolved by forwarding, also called bypassing, short-circuiting.**
- **Data Hazards Requiring Stalls: In some cases, data hazards can not be handled by bypassing.**

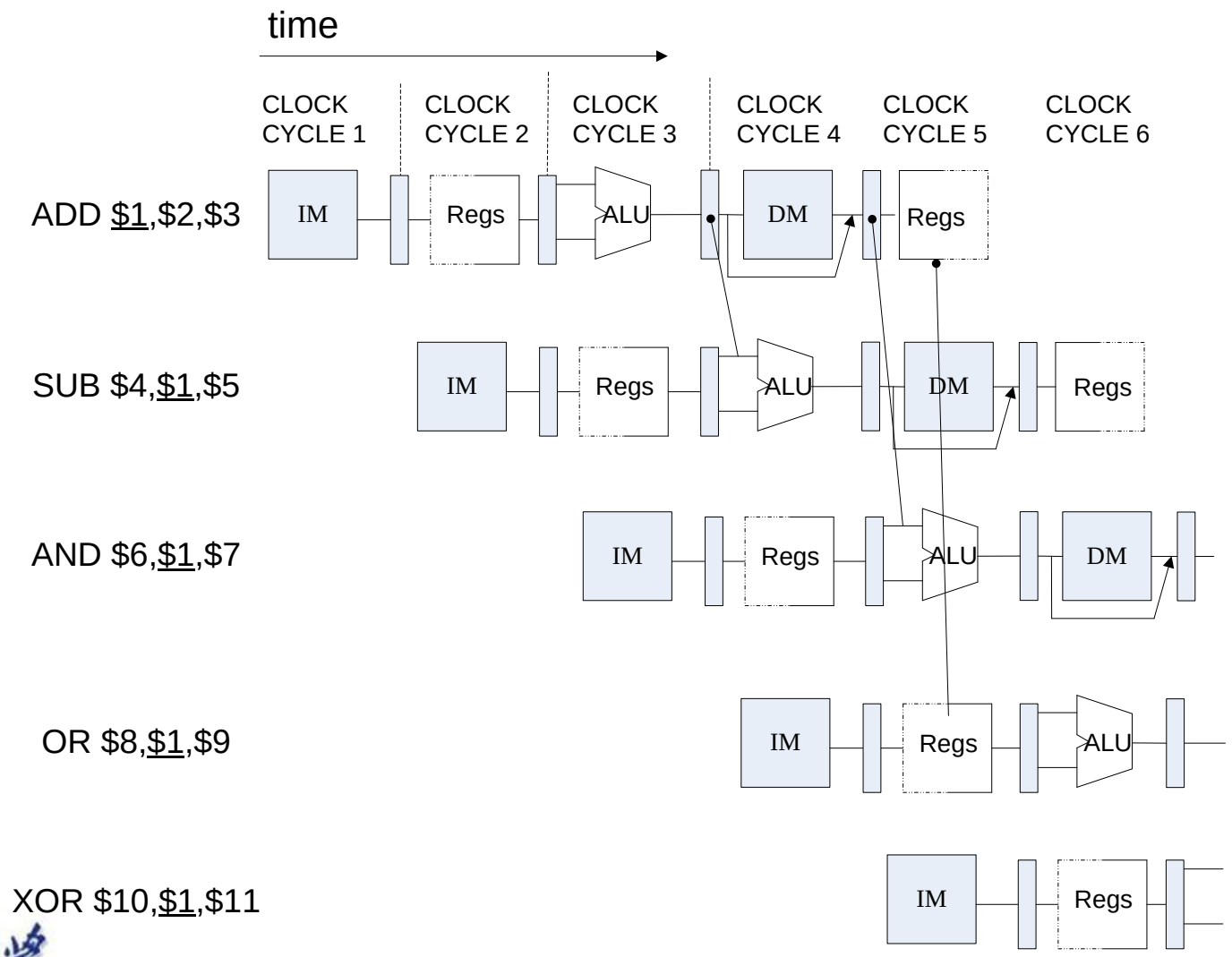
Instruction Demo



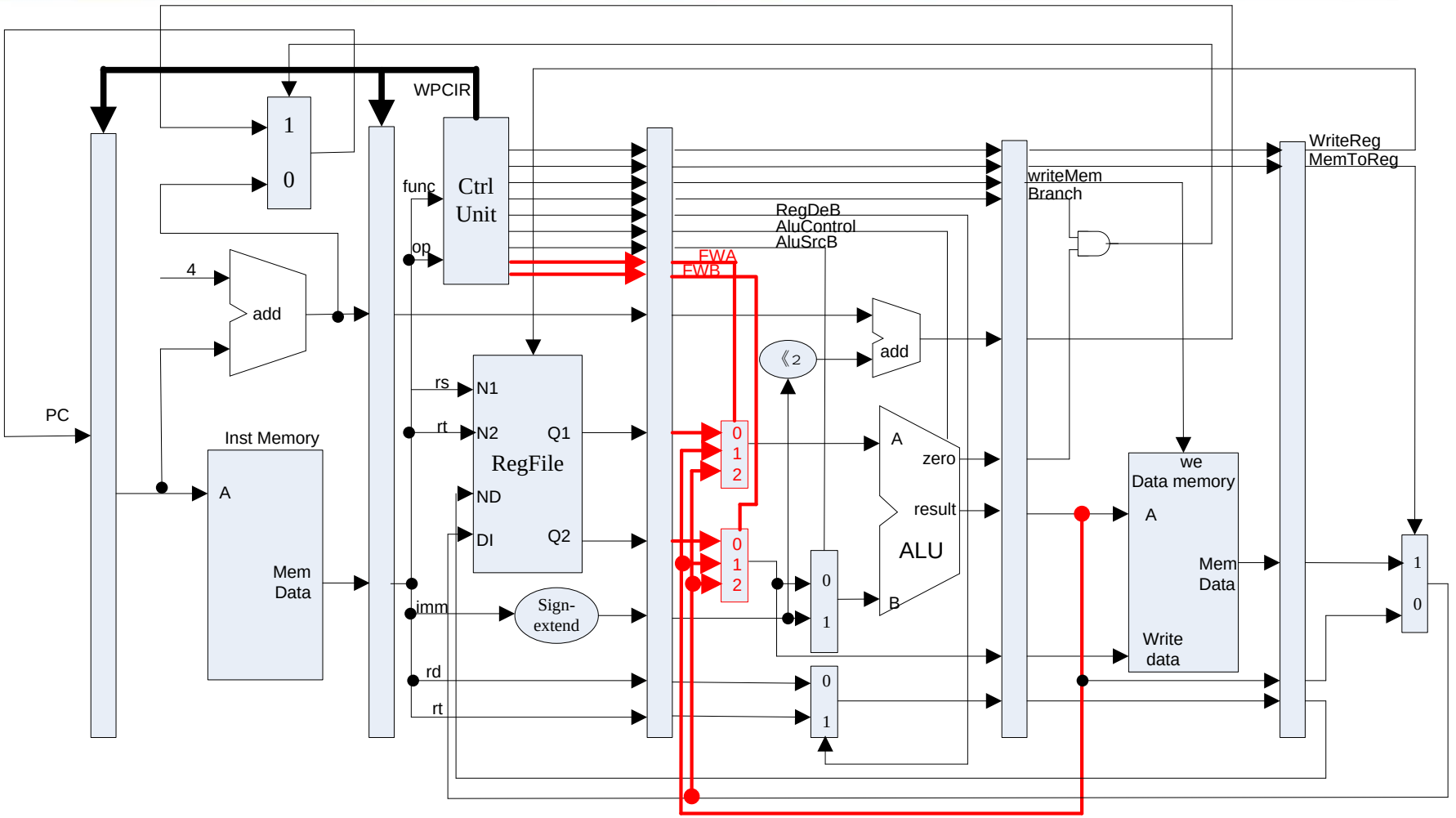
Data Hazard Causes Stalls



Pipeline Forward to Avoid the Data hazard



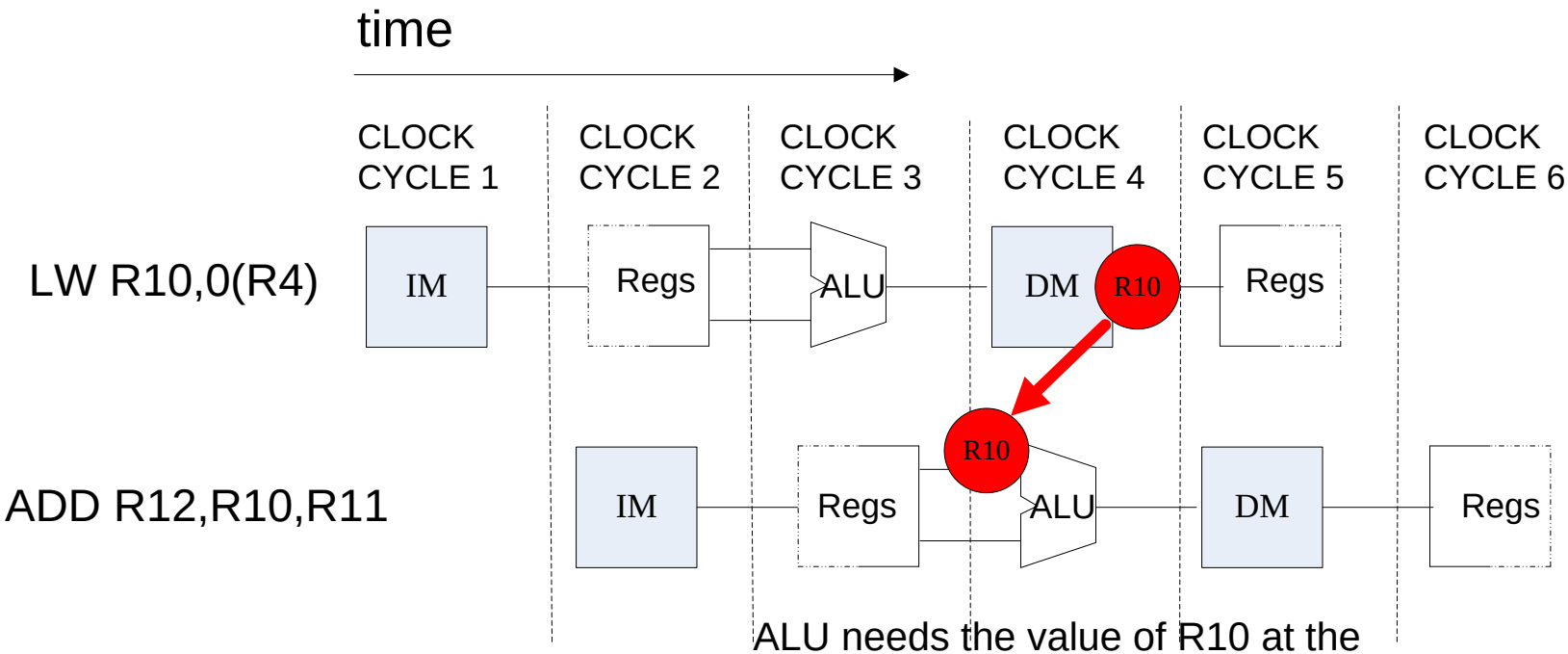
Datapath with Bypass Unit



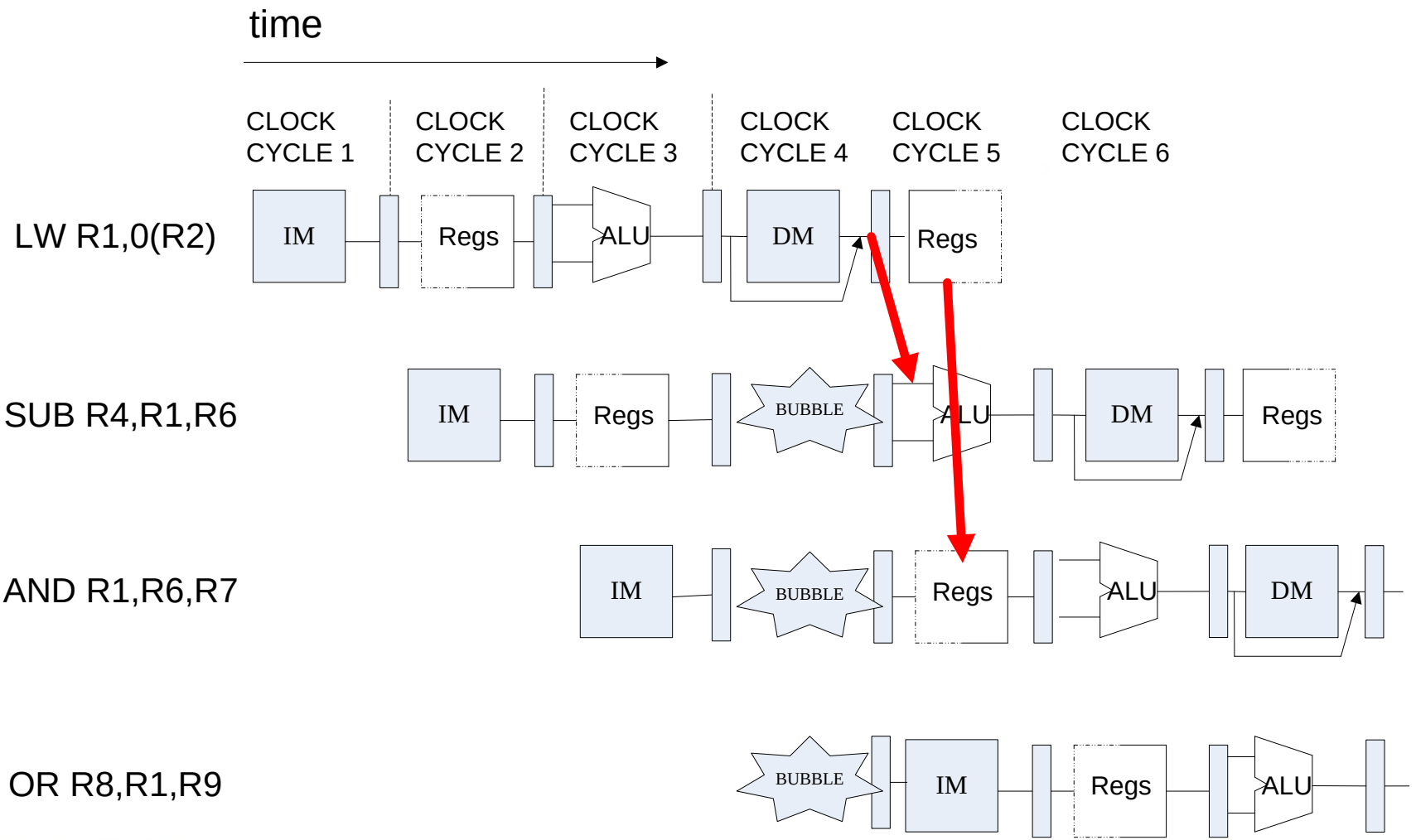
In Which Conditions the Pipeline Forward

```
if(MEM.WriteReg
    and(MEM.RegisterRd!=0)
    and(MEM.RegisterRd==EXE.RegisterRs)) ForwardA=01
if(MEM.WriteReg
    and(MEM.RegisterRd!=0)
    and(MEM.RegisterRd==EXE.RegisterRt)) ForwardB=01
if(WB.WriteReg
    and(WB.RegisterRd!=0)
    and(MEM.RegisterRd==EXE.RegisterRs)
    and(WB.RegisterRd==EXE.RegisterRs)) ForwardA=10
if(WB.WriteReg
    and(WB.RegisterRd!=0)
    and(MEM.RegisterRd==EXE.RegisterRt)
    and(WB.RegisterRd==EXE.RegisterRt)) ForwardB=10
```

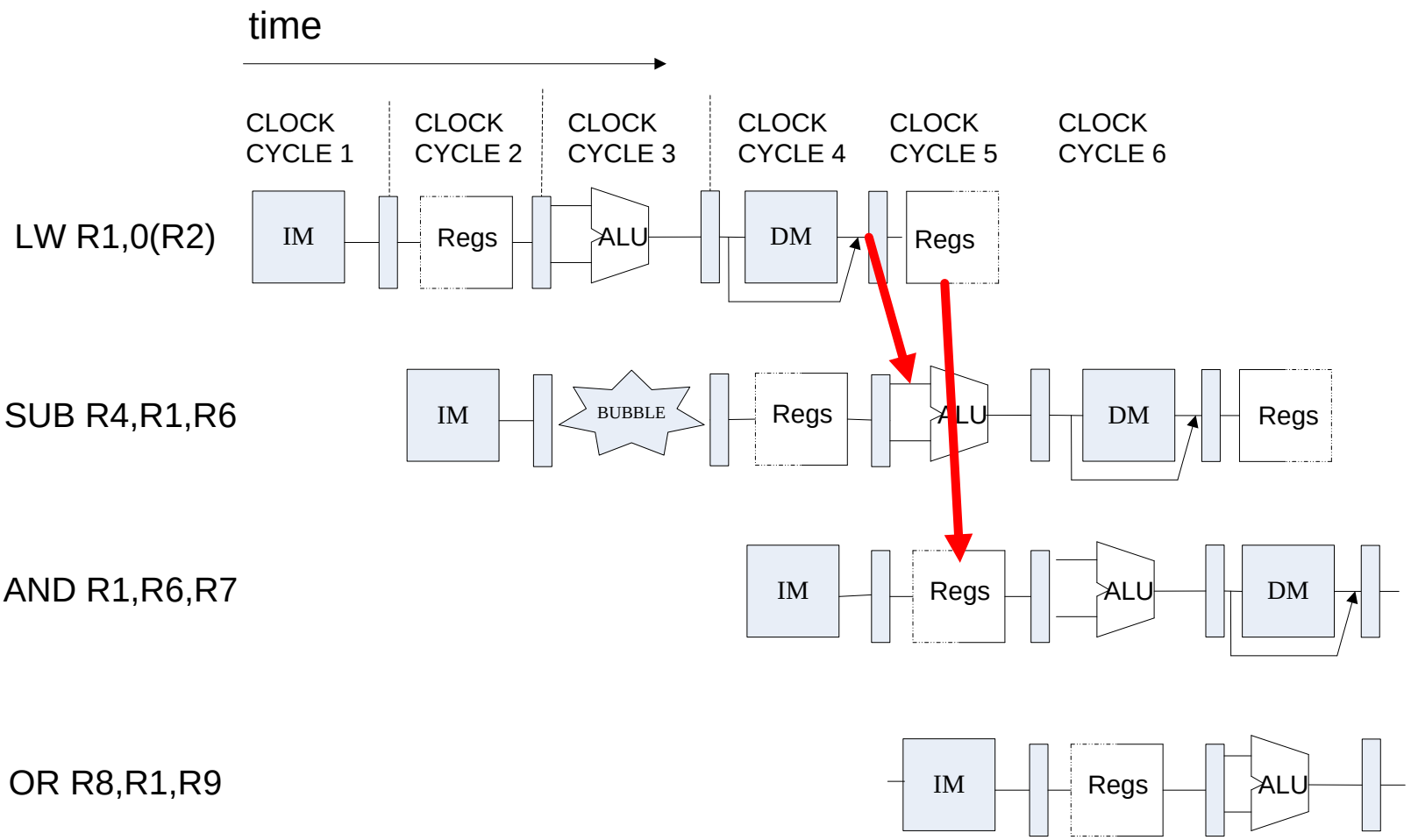
Condition in Which Bypass Unit doesn't work



Pipeline Stalls



Pipeline stalls at ID Stage



Condition in which Pipeline Forwards and stalls

```
…
assign AfromEx = …              //ALUOp
assign BfromEx = …              //ALUOp
assign AfromMem = …             //ALUOp + LW
assign BfromMem = …             //ALUOp + LW
assign AfromExLW = …            //与 if_inst 比
assign BfromExLW = …            //与 if_inst 比
…
assign cu_fwda[1:0] = (AfromEx == 1)? 2'b01 :((AfromMem == 1)?2'b10:2’b00);
assign cu_fwdb[1:0] = (BfromEx == 1)? 2'b01 :((BfromMem == 1)?2'b10:2'b00);
…
assign stall = AfromExLW || BfromExLW;
…
```

Pipelined CPU Top Module

- module top (input wire CCLK, BTN3, BTN2, input wire [3:0]SW,
  output wire LED, LCDE, LCDRS, LCDRW, output wire [3:0]LCDDAT);
- assign pc [31:0] = if_npc[31:0];
- if_stage x_if_stage(BTN3, rst, pc, mem_pc, mem_branch, id_wpcir, …
- IF_ins_type, IF_ins_number,ID_ins_type,ID_ins_number);
- id_stage x_id_stage(BTN3, rst, if_inst, if_pc4, wb_destR,…,
- EX_ins_type, EX_ins_number, id_FWA, id_FWB);
- ex_stage x_ex_stage(BTN3, id_imm, id_inA, id_inB, id_wreg, ..
- id_FWA, id_FWB,mem_aluR, wb_dest, … , MEM_ins_number);
- mem_stage x_mem_stage(BTN3, ex_destR, ex_inB, ex_aluR, …
- mem_aluR, ... , WB_ins_type, WB_ins_number);
- wb_stage x_wb_stage(BTN3, mem_destR, mem_aluR, …
- wb_dest, …, OUT_ins_type, OUT_ins_number);

Observation Info

- **Input**
  - West Button: Step execute
  - South Button: Reset
  - 4 Slide Button: Register Index
- **Output**
  - 0-7 Character of First line: Instruction Code
  - 8 of First line : Space
  - 9-10 of First line : Clock Count
  - 11 of First line : Space
  - 12-15 of First line : Register Content
  - Second line : “stage name”/number/type

  stage name: 1-”f”, 2-”d”, 3-”e”, 4-”m”, 5-”w”

Program for verification

No	Instruction	Bin Code	Address	Inst. Type
1	lw r1, $20(r0)	0x8c01_0014	0	6
2	lw r2, $21(r0)	0x8c02_0015	1	6
3	add r3, r1, r2	0x0022_1820	2	1
4	add r2,r0,r0	0x0000_1020	3	1
5	sub r4, r1, r3	0x0023_2022	4	2
6	and r5, r3, r4	0x0064_2824	5	3
7	nor r6, r4, r5	0x0085_3027	6	5
8	sw r6, $22(r0)	0xac06_0016	7	7
9	beq r6,r7,-8	0x10c7_fff8	8	8

Thanks!

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